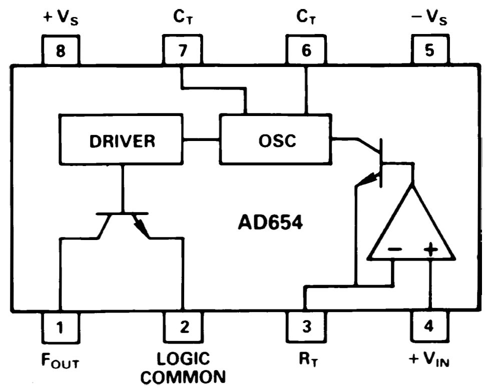
Low Cost Monolithic Voltage-to-Frequency Converter

AD654

FEATURES
Low Cost
Single or Dual Supply, 5 V to 36 V, ±5 V to ±18 V
Full-Scale Frequency Up to 500 kHz
Minimum Number of External Components Needed
Versatile Input Amplifier
Positive or Negative Voltage Modes
Negative Current Mode
High Input Impedance, Low Drift
Low Power: 2.0 mA Quiescent Current
Low Offset: 1 mV

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD654 is a monolithic V/F converter consisting of an input amplifier, a precision oscillator system, and a high current output stage. A single RC network is all that is required to set up any full scale (FS) frequency up to 500 kHz and any FS input voltage up to ±30 V. Linearity error is only 0.03% for a 250 kHz FS, and operation is guaranteed over an 80 dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±50 ppm/°C. The AD654 operates from a single supply of 5 V to 36 V and consumes only 2.0 mA quiescent current.

The low drift (4 μV/°C typ) input amplifier allows operation directly from small signals such as thermocouples or strain gauges while offering a high (250 MΩ) input resistance. Unlike most V/F converters, the AD654 provides a square-wave output, and can drive up to 12 TTL loads, optocouplers, long cables, or similar loads.

PRODUCT HIGHLIGHTS

1. Packaged in both an 8-pin mini-DIP and an 8-pin SOIC package, the AD654 is a complete V/F converter requiring only an RC timing network to set the desired full-scale frequency and a selectable pullup resistor for the open-collector output stage. Any full scale input voltage range from 100 mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of the timing resistor. The full-scale frequency is then set by the timing capacitor from the simple relationship, $f = V/10\ RC$.
2. A minimum number of low cost external components are necessary. A single RC network is all that is required to set up any full scale frequency up to 500 kHz and any full-scale input voltage up to ±30 V.
3. Plastic packaging allows low cost implementation of the standard VFC applications: A/D conversion, isolated signal transmission, F/V conversion, phase-locked loops, and tuning switched-capacitor filters.
4. Power supply requirements are minimal; only 2.0 mA of quiescent current is drawn from the single positive supply from 4.5 volts to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ –4) volts. Negative inputs can easily be connected for below ground operation.
5. The versatile open-collector output stage can sink more than 10 mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

REV. A

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AD654–SPECIFICATIONS (T_A = +25°C and V_S (total) = 5 V to 16.5 V, unless otherwise noted. All testing done@ V_S = +5 V.)

Model	AD654JN/JR Min	Typ	Max	Units
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0		500	kHz
Nonlinearity[1]				
f_{MAX} = 250 kHz		0.06	**0.1**	%
f_{MAX} = 500 kHz		0.20	0.4	%
Full-Scale Calibration Error				
C = 390 pF, I_{IN} = 1.000 mA	**–10**		**10**	%
vs. Supply (f_{MAX} ≤ 250 kHz)				
V_S = +4.75 V to +5.25 V		0.20	**0.40**	%/V
V_S = +5.25 V to +16.5 V		0.05	**0.10**	%/V
vs. Temp (0°C to +70°C)		50		ppm/°C
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0		(+V_S – 4)	V
Dual Supply	–V_S		(+V_S – 4)	V
Input Bias Current				
(Either Input)		30	**50**	nA
Input Offset Current		5		nA
Input Resistance (Noninverting)		250		MΩ
Input Offset Voltage		0.5	**1.0**	mV
vs. Supply				
V_S = +4.75 V to +5.25 V		0.1	**0.25**	mV/V
V_S = +5.25 V to +16.5 V		0.03	**0.1**	mV/V
vs. Temp (0°C to +70°C)		4		µV/°C
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"[2]				
V_{OUT} = 0.4 V max, +25°C	**10**	20		mA
V_{OUT} = 0.4 V max, 0°C to +70°C	5	10		mA
Output Leakage Current in Logic "1"		10	**100**	nA
0°C to +70°C		50	500	nA
Logic Common Level Range	–V_S		(+V_S – 4)	V
Rise/Fall Times (C_T = 0.01 µF)				
I_{IN} = 1 mA		0.2		µs
I_{IN} = 1 µA		1		µs
POWER SUPPLY				
Voltage, Rated Performance	4.5		16.5	V
Voltage, Operating Range				
Single Supply	4.5		36	V
Dual Supply	±5		±18	V
Quiescent Current				
V_S (Total) = 5 V		1.5	**2.5**	mA
V_S (Total) = 30 V		2.0	**3.0**	mA
TEMPERATURE RANGE				
Operating Range	–40		+85	°C
PACKAGE OPTIONS[3]				
SOIC (R-8)		AD654JR		
Plastic DIP (N-8)		AD654JN		

NOTES

[1]At f_{MAX} = 250 kHz; R_T = 1 kΩ, C_T = 390 pF, I_{IN} = 0 mA–1 mA.
f_{MAX} = 500 kHz; R_T = 1 kΩ, C_T = 200 pF, I_{IN} = 0 mA–1 mA.

[2]The sink current is the amount of current that can flow into Pin 1 of the AD654 while maintaining a maximum voltage of 0.4 V between Pin 1 and Logic Common.

[3]N = Plastic DIP; R = SOIC.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATING

Total Supply Voltage $+V_S$ to $-V_S$ . . . . 36 V
Maximum Input Voltage
(Pins 3, 4) to $-V_S$ . . . . –300 mV to $+V_S$
Maximum Output Current
Instantaneous . . . . 50 mA
Sustained . . . . 25 mA
Logic Common to $-V_S$ . . . . –500 mV to $(+V_S -4)$
Storage Temperature Range . . . . –65°C to +150°C

CIRCUIT OPERATION

The AD654's block diagram appears in Figure 1. A versatile operational amplifier serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full-scale input voltage, a 1 mA drive current is delivered to the current-to-frequency converter (an astable multivibrator). The drive current provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 100 nA to 2 mA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a level other than $-V_S$.

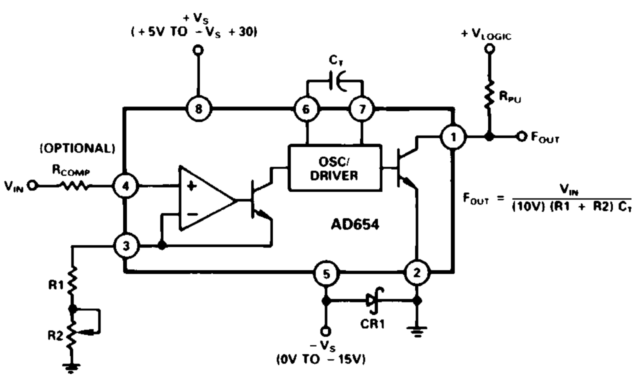


Figure 1. Standard V-F Connection for Positive Input Voltages

V/F CONNECTION FOR POSITIVE INPUT VOLTAGES

In the connection scheme of Figure 1, the input amplifier presents a very high (250 MΩ) impedance to the input voltage, which is converted into the proper drive current by the scaling resistors at Pin 3. Resistors R1 and R2 are selected to provide a 1 mA full-scale current with enough trim range to accommodate the AD654's 10% FS error and the components' tolerances. Full-scale currents other than 1 mA can be chosen, but linearity will be reduced; 2 mA is the maximum allowable drive. The AD654's positive input voltage range spans from $-V_S$ (ground in sink supply operation) to four volts below the positive supply. Power supply rejection degrades as the input exceeds $(+V_S - 3.75\ V)$ and at $(+V_S - 3.5\ V)$ the output frequency goes to zero.

As indicated by the scaling relationship in Figure 1, a 0.01 µF timing capacitor will give a 10 kHz full-scale frequency, and 0.001 µF will give 100 kHz with a 1 mA drive current. Good V/F linearity requires the use of a capacitor with low dielectric absorption (DA), while the most stable operation over temperature calls for a component having a small tempco. Polystyrene, polypropylene, or Teflon* capacitors are preferred for tempco and dielectric absorption; other types will degrade linearity. The capacitor should be wired very close to the AD654. In Figure 1, Schottky diode CR1 (MBD101) prevents logic common from dropping more than 500 mV below $-V_S$. This diode is not required if $-V_S$ is equal to logic common.

*Teflon is a trademark of E.I. Du Pont de Nemours & Co.

V/F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

The AD654 can accommodate a wide range of negative input voltages with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance because the signal source must supply the 1 mA FS drive current. However, large negative voltages beyond the supply can be handled easily by modifying the scaling resistors appropriately. If the input is a true current source, R1 and R2 are not used. Again, diode CR1 prevents latch-up by insuring Logic Common does not drop more than 500 mV below $-V_S$. The clamp diode (MBD101) protects the AD654 input from "below $-V_S$" inputs.

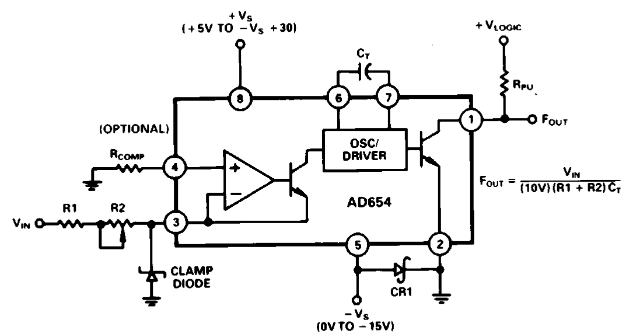


Figure 2. V-F Connections for Negative Input Voltages or Current

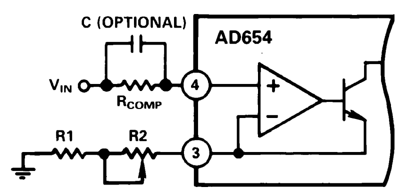


Figure 3a. Bias Current Compensation—Positive Inputs

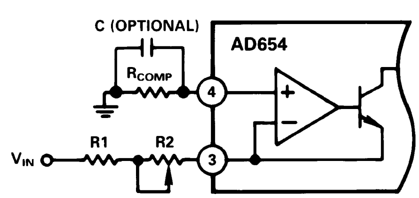


Figure 3b. Bias Current Compensation—Negative Inputs

If the AD654's 1 mV offset voltage must be trimmed, the trim must be performed external to the device. Figure 3c shows an optional connection for positive inputs in which R_{OFF1} and R_{OFF2} add a variable resistance in series with R_T. A variable source of ±0.6 V applied to R_{OFF1} then adjusts the offset ±1 mV. Similarly, a ±0.6 V variable source is applied to R_{OFF} in Figure 3d to trim offset for negative inputs. The ±0.6 V bipolar source could simply be an AD589 reference connected as shown in Figure 3e.

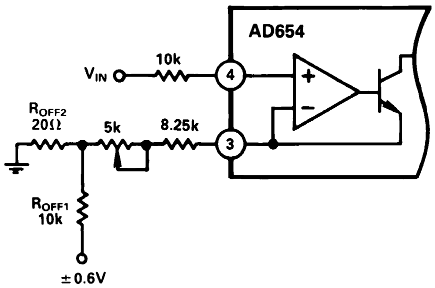


Figure 3c. Offset Trim Positive Input (10 V FS)

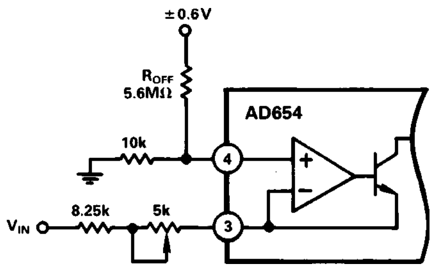


Figure 3d. Offset Trim Negative Input (–10 V FS)

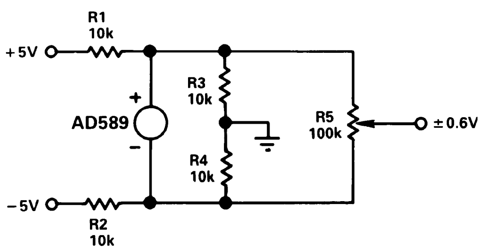


Figure 3e. Offset Trim Bias Network

FULL-SCALE CALIBRATION

Full-scale trim is the calibration of the circuit to produce the desired output frequency with a full-scale input applied. In most cases this is accomplished by adjusting the scaling resistor R_T. Precise calibration of the AD654 requires the use of an accurate voltage standard set to the desired FS value and an accurate frequency meter. A scope is handy for monitoring output waveshape. Verification of converter linearity requires the use of a switchable voltage source or DAC having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. Since each AD654 is factory tested for linearity, it is unnecessary for the end-user to perform this tedious and time consuming test on a routine basis.

Sufficient FS calibration trim range must be provided to accommodate the worst-case sum of all major scaling errors. This includes the AD654's 10% full-scale error, the tolerance of the fixed scaling resistor, and the tolerance of the timing capacitor. Therefore, with a resistor tolerance of 1% and a capacitor tolerance of 5%, the fixed part of the scaling resistor should be a maximum of 84% of nominal, with the variable portion selected to allow 116% of the nominal.

If the input is in the form of a negative current source, the scaling resistor is no longer required, eliminating the capability of trimming FS frequency in this fashion. Since it is usually not practical to smoothly vary the capacitance for trimming purposes, an alternative scheme such as the one shown in Figure 4 is needed. Designed for a FS of 1 mA, this circuit divides the input into two current paths. One path is through the 100 Ω

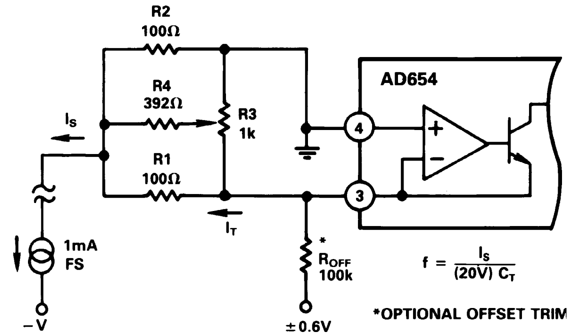


Figure 4. Current Source FS Trim

resistor R1, and flowing into Pin 3; it constitutes the signal current I_T to be converted. The second path, through another 100 Ω resistor R2, carries the same nominal current. Two equal valued resistors offer the best overall stability, and should be either 1% discrete film units, or a pair from a common array.

Since the 1 mA FS input current is divided into two 500 µA legs (one to ground and one to Pin 3), the total input signal current (I_S) is divided by a factor of two in this network. To achieve the same conversion scale factor, C_T must be reduced by a factor of two. This results in a transfer unique to this hookup:

$$f = \frac{I_S}{(20\ V)\ C_T}$$

For calibration purposes, resistors R3 and R4 are added to the network, allowing a ±15% trim of scale factor with the values shown. By varying R4's value the trim range can be modified to accommodate wider tolerance components or perhaps the calibration tolerance on a current output transducer such as the AD592 temperature sensor. Although the values of R1–R4 shown are valid for 1 mA FS signals only, they can be scaled upward proportionately for lower FS currents. For instance, they should be increased by a factor of ten for a FS current of 100 µA.

In addition to the offsets generated by the input amplifier's bias and offset currents, an offset voltage induced parasitic current arises from the current fork input network. These effects are minimized by using the bias current compensation resistor R_{OFF} and offset trim scheme shown in Figure 3e.

Although device warm-up drifts are small, it is good practice to allow the devices operating environment to stabilize before trim, and insure the supply, source and load are appropriate. If provision is made to trim offset, begin by setting the input to 1/10,000 of full scale. Adjust the offset pot until the output is 1/10,000 of full scale (for example, 25 Hz for a FS of 250 kHz). This is most easily accomplished using a frequency meter connected to the output. The FS input should then be applied and the gain pot should be adjusted until the desired FS frequency is indicated.

INPUT PROTECTION

The AD654 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions. Thus $+V_{IN}$ and R_T pins should not be driven more than 300 mV below $-V_S$. Likewise, Logic Common should not drop more than 500 mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. In addition to the diode shown in Figures 1 and 2 protecting Logic Common, a second Schottky diode (MBD101) can protect the AD654's inputs from "below $-V_S$" inputs as

shown in Figure 5. It is also desirable not to drive $+V_{IN}$ and R_T above $+V_S$. In operation, the converter will exhibit a zero output for inputs above ($+V_S$ – 3.5 V). Also, control currents above 2 mA will increase nonlinearity.

The AD654's 80 dB dynamic range guarantees operation from a control current of 1 mA (nominal FS) down to 100 nA (equivalent to 1 mV to 10 V FS). Below 100 nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to input. For example, when scaled to accept an FS input of 1 V, the –80 dB level is only 100 µV, so when the mean input is only 60 dB below FS (1 mV), noise spikes of 0.9 mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter or a guard ring around the R_T pin. The filter can be assembled using the bias current compensation resistor discussed in the previous section. For an FS of 10 kHz, a single-pole filter with a time constant of 100 ms will be suitable, but the optimum configuration will depend on the application and the type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100 nA full integration of additive input noise occurs. Like the inputs, the capacitor terminals are sensitive to interference from other signals. The timing capacitor should be located as close as possible to the AD654 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100 Ω) in the supply lines to provide a measure of decoupling

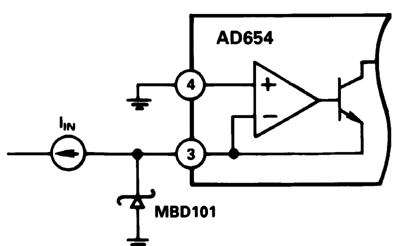


Figure 5. Input Protection

between the various circuits in the system. Ceramic capacitors of 0.1 µF to 1.0 µF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD654. A proper ground scheme appears in Figure 6.

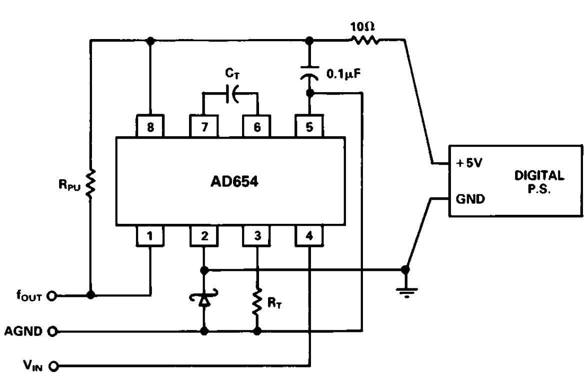


Figure 6. Proper Ground Scheme

OUTPUT INTERFACING CONSIDERATION

The output stage's design allows easy interfacing to all digital logic families. The output NPN transistor's emitter and collector are both uncommitted. The emitter can be tied to any voltage between $–V_S$ and 4 volts below $+V_S$, and the open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can sink over 10 mA at a maximum saturation voltage of 0.4 V. The stage limits the output current at 25 mA and can handle this limit indefinitely without damaging the device.

NONLINEARITY SPECIFICATION

The preferred method of specifying nonlinearity error is in terms of maximum deviation from the ideal relationship after calibrating the converter at full scale. This error will vary with the full scale frequency and the mode of operation. The AD654 operates best at a 150 kHz full-scale frequency with a negative voltage input; the linearity is typically within 0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the Specifications Table. Typical linearity at various temperatures is shown in Figure 7.

TWO-WIRE TEMPERATURE-TO-FREQUENCY CONVERSION

Figure 8 shows the AD654 in a two-wire temperature-to-frequency conversion scheme. The twisted pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation.

The positive supply line is fed to the remote V/F through a 140 Ω resistor. This resistor is selected such that the quiescent current of the AD654 will cause less than one V_{BE} to be dropped.

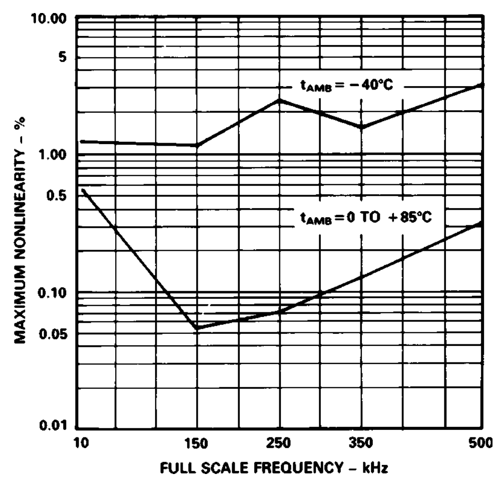


Figure 7. Typical Nonlinearities at Different Full-Scale Frequencies

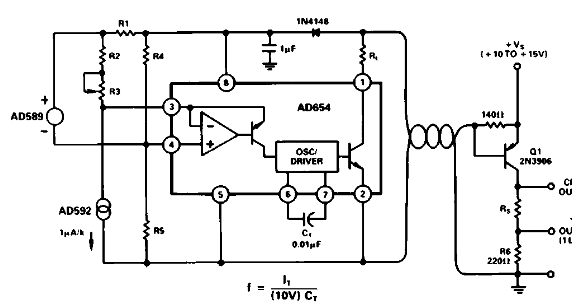


Figure 8. Two-Wire Temperature-to-Frequency Converter

As the V/F oscillates, additional switched current is drawn through R_L when Pin 1 goes low. The peak level of this additional current causes Q1 to saturate, and thus regenerates the AD654's output square wave at the collector. The supply voltage to the AD654 then consists of a dc level, less the resistive line drop, plus a one V_{BE} p-p square wave at the output frequency of the AD654. This ripple is reduced by the diode/capacitor combination.

To set up the receiver circuit for a given voltage, the R_S and R_L resistances are selected as shown in Table I. CMOS logic stages can be driven directly from the collector of Q1, and a single TTL load can be driven from the junction of R_S and R6.

Table I.

$+V_S$	R_S	R_L
10 V	270 Ω	1.8k
15 V	680 Ω	2.7k

Table II.

	$(+V_S)$	R1	R2	R3	R4	R5	
K	10 V	–	–	–	100k	127k	F = 10 Hz/K
	15 V	–	–	–	100k	127k	
°C	10 V	6.49k	4.02k	1k	95.3k	22.6k	F = 10 Hz/°C
	15 V	12.7k	4.02k	1k	78.7k	36.5k	
°F	10 V	6.49k	4.42k	1k	154k	22.6k	F = 5.55 Hz/°F
	15 V	12.7k	4.42k	1k	105k	36.5k	

At the V/F end, the AD592C temperature transducer is interfaced with the AD654 in such a manner that the AD654 output frequency is proportional to temperature. The output frequency can be sealed and offset from K to °C or °F using the resistor values shown in Table II. Since temperature is the parameter of interest, an NPO ceramic capacitor is used as the timing capacitor for low V/F TC.

When scaling per K, resistors R1–R3 and the AD589 voltage reference are not used. The AD592 produces a 1 µA/K current output which drives Pin 3 of the AD654. With the timing capacitor of 0.01 µF this produces an output frequency scaled to 10 Hz/K. When scaling per °C and °F, the AD589 and resistors R1–R3 offset the drive current at Pin 3 by 273.2 µA for scaling per °C and 255.42 µA for scaling per °F. This will result in frequencies sealed at 10 Hz/°C and 5.55 Hz/°F, respectively.

OPTOISOLATOR COUPLING

A popular method of isolated signal coupling is via optoelectronic isolators, or optocouplers. In this type of device, the signal is coupled from an input LED to an output photo-transistor, with light as the connecting medium. This allows dc to be transmitted, is extremely useful in overcoming ground loop problems between equipment, and is applicable over a wide range of speeds and power.

Figure 9 shows a general purpose isolated V/F circuit using a low cost 4N37 optoisolator. A +5 V power supply is assumed for both the isolated (+5 V isolated) and local (+5 V local) supplies. The input LED of the isolator is driven from the collector output of the AD654, with a 9 mA current level established by R1 for high speed, as well as for a 100% current transfer ratio.

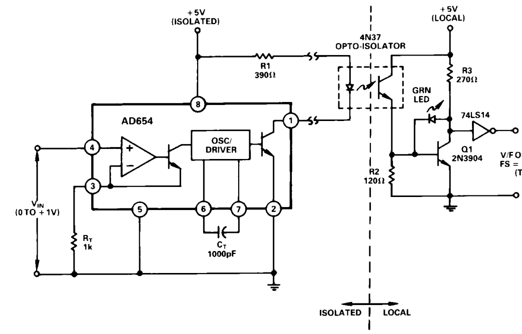


Figure 9. Optoisolator Interface

At the receiver side, the output transistor is operated in the photo-transistor mode; that is with the base lead (Pin 6) open. This allows the highest possible output current. For reasonable speed in this mode, it is imperative that the load impedance be as low as possible. This is provided by the single transistor stage current-to-voltage converter, which has a dynamic load impedance of less than 10 ohms and interfaces with TTL at the output.

USING A STAND-ALONE FREQUENCY COUNTER/LED DISPLAY DRIVER FOR VOLTMETER APPLICATIONS

Figure 10 shows the AD654 used with a stand-alone frequency counter/LED display driver. With C_T = 1000 pF and R_T = 1 kΩ the AD654 produces an FS frequency of 100 kHz when V_{IN} = +1 V. This signal is fed into the ICM7226A, a universal counter system that drives common anode LEDs. With the FUNCTION pin tied to D1 through a 10 kΩ resistor the ICM7226A counts the frequency of the signal at A_{IN}. This count period is selected by the user and can be 10 ms, 100 ms, 1s, or 10 seconds, as shown on Pin 21. The longer the period selected, the more resolution the count will have. The ICM7226A then displays the frequency on the LEDs, driving them directly as shown. Refreshing of the LEDs is handled automatically by the ICM7226. The entire circuit operates on a single +5 V supply and gives a meter with 3, 4, or 5 digit resolution.

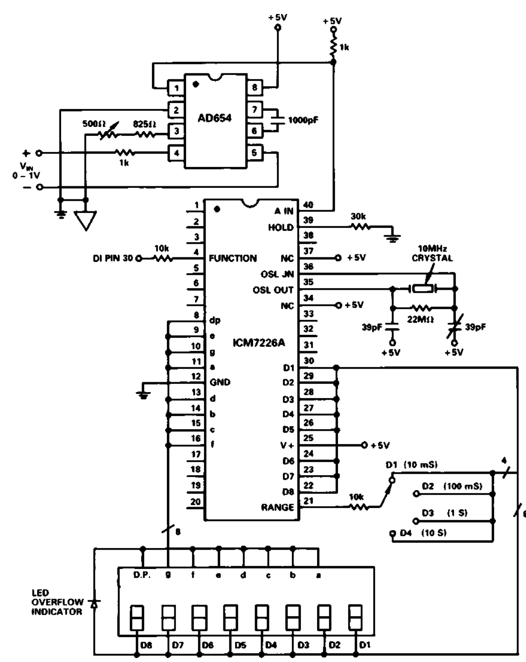


Figure 10. AD654 With Stand-Alone Frequency Counter/LED Display Driver

Longer count periods not only result in the count having more resolution, they also serve as an integration of noisy analog signals. For example, a normal-mode 60 Hz sine wave riding on the input of the AD654 will result in the output frequency increasing on the positive half of the sine wave and decreasing on the negative half of the sine wave. This effect is cancelled by selecting a count period equal to an integral number of noise signal periods. A 100 ms count period is effective because it not only has an integral number of 60 Hz cycles (6), it also has an integral number of 50 Hz cydes (5). This is also true of the 1 second and 10 second count period.

AD654-BASED ANALOG-TO-DIGITAL CONVERSION USING A SINGLE CHIP MICROCOMPUTER

The AD654 can serve as an analog-to-digital converter when used with a single component microcomputer that has an interval timer/event counter such as the 8048. Figure 11 shows the AD654, with a full-scale input voltage of +1 V and a full-scale output frequency of 100 kHz, connected to the timer/counter input Pin T1 of the 8048. Such a system can also operate on a single +5 V supply.

The 8748 counter is negative edge triggered; after the STRT CNT instruction is executed subsequent high to low transitions on T1 increment the counter. The maximum rate at which the counter may be incremented is once per three instruction cycles; using a 6 MHz crystal, this corresponds to once every 7.5 µs, or a maximum frequency of 133 kHz. Because the counter overflows every 256 counts (8 bits), the timer interrupt is enabled. Each overflow then causes a jump to a subroutine where a register is incremented. After the STOP TCNT instruction is executed, the number of overflows that have occurred will be the number in this register. The number in this register multiplied by 256 plus the number in the counter will be the total number of negative edges counted during the count period. The count period is handled simply by decrementing a register the number of times necessary to correspond to the desired count time. After the register has been decremented the required number of times the STOP TCNT instruction is executed.

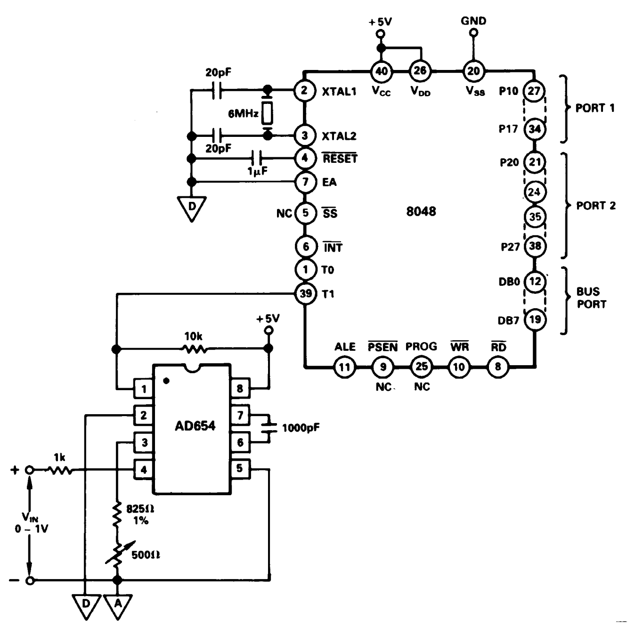


Figure 11. AD654 VFC as an ADC

The total number of negative edges counted during the count period is proportional to the input voltage. For example, if a 1 V full-scale input voltage produces a 100 kHz signal and the count period is 100 ms, then the total count will be 10,000. Scaling from this maximum is then used to determine the input voltage, i.e., a count of 5000 corresponds to an input voltage of 0.5 V. As with the ICM7226, longer count times result in counts having more resolution; and they result in the integration of noisy analog signals.

FREQUENCY DOUBLING

Since the AD654's output is a square-wave rather than a pulse train, information about the input signal is carried on both halves of the output waveform. The circuit in Figure 12 converts the output into a pulse train, effectively doubling the output frequency, while preserving the better low frequency linearity of the AD654. This circuit also accommodates an input voltage that is greater than the AD654 supply voltage.

Resistors R1–R3 are used to scale the 0 V to +10 V input voltage down to 0 V to +1 V as seen at Pin 4 of the AD654. Recall that V_{IN} must be less than V_{SUPPLY} –4 V, or in this case less than 1 V. The timing resistor and capacitor are selected such that this 0 V to +1 V signal seen at Pin 4 results in a 0 kHz to 200 kHz output frequency.

The use of R4, C1 and the XOR gate doubles this 200 kHz output frequency to 400 kHz. The AD654 output transistor is basically used as a switch, switching capacitor C1 between a charging mode and a discharging mode of operation. The voltages

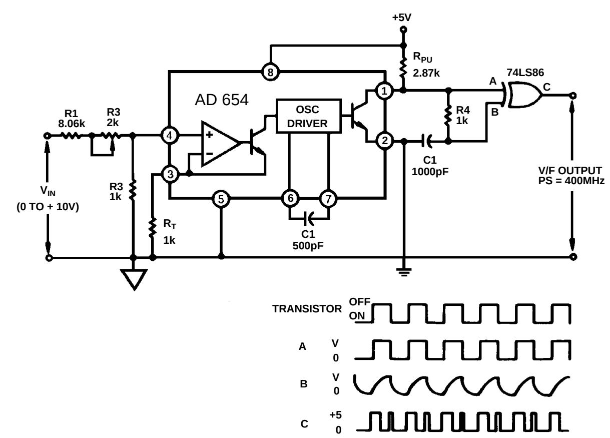


Figure 12. Frequency Doubler

seen at the input of the 74LS86 are shown in the waveform diagram. Due to the difference in the charge and discharge time constants, the output pulse widths of the 74LS86 are not equal. The output pulse is wider when the capacitor is charging due to its longer rise time than fall time. The pulses should therefore be counted on their rising, rather than falling, edges.

OPERATION AT HIGHER OUTPUT FREQUENCIES

Operation of the AD654 via the conventional output (Pins 1 and 2) is speed limited to approximately 500 kHz for reasons of TTL logic compatibility. Although the output stage may become speed limited, the multivibrator core itself is able to oscillate to 1 MHz or more. The designer may take advantage of this feature in order to operate the device at frequencies in excess of 500 kHz.

Figure 13 illustrates this with a circuit offering 2 MHz full scale. In this circuit the AD654 is operated at a full scale (FS) of 1 mA, with a C_T of 100 pF. This achieves a basic device FS frequency of 1 MHz across C_T. The P channel JFETs, Q1 and Q2, buffer the differential timing capacitor waveforms to a low impedance level where the push-pull signal is then ac coupled to the high speed comparator A2. Hysteresis is used, via R7, for non-ambiguous switching and to eliminate the oscillations which would otherwise occur at low frequencies.

The net result of this is a very high speed circuit which does not compromise the AD654 dynamic range. This is a result of the FET buffers typically having only a few pA of bias current. The high end dynamic range is limited, however, by parasitic package and layout capacitances in shunt with C_T, as well as those from each node to ac ground. Minimizing the lead length between A2–6/A2–7 and Q1/Q2 in PC layout will help. A ground plane

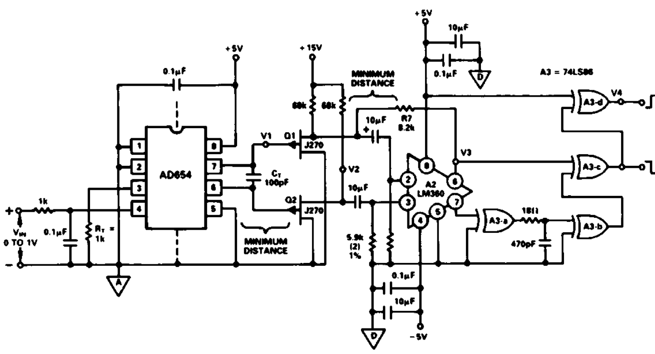


Figure 13. 2 MHz, Frequency Doubling V/F

will also help stability. Figure 14 shows the waveforms V1–V4 found at the respective points shown in Figure 13.

The output of the comparator is a complementary square wave at 1 MHz FS. Unlike pulse train output V/F converters, each half-cycle of the AD654 output conveys information about the input. Thus it is possible to count edges, rather than full cycles of the output, and double the effective output frequency. The XOR gate following A2 acts as an edge detector producing a short pulse for each input state transition. This effectively doubles the V/F FS frequency to 2 MHz. The final result is a 1 V full-scale input V/F with a 2 MHz full-scale output capability; typical nonlinearity is 0.5%.

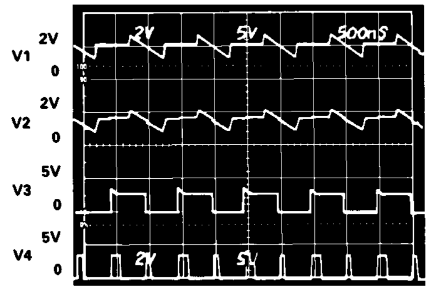
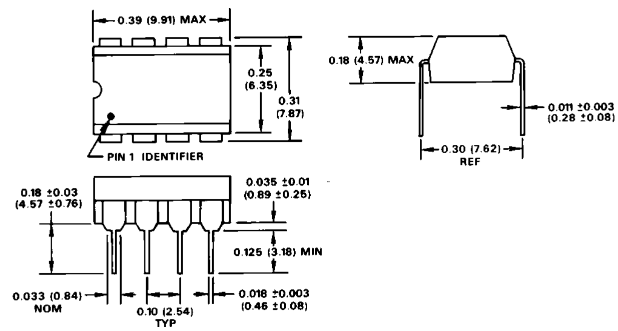


Figure 14. Waveforms of 2 MHz Frequency Doubler

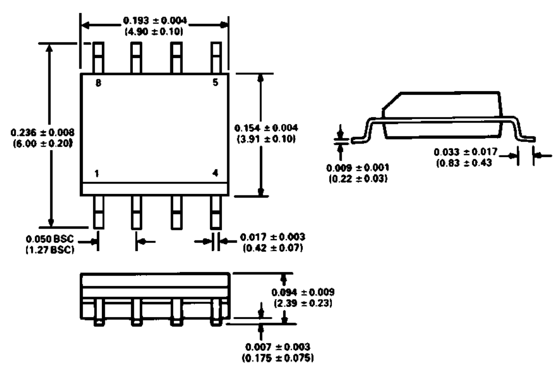
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Pin Plastic DIP



8-Pin SOIC



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